AMENDMENTS TO THE CLAIMS

(COMPLIANT WITH THE REVISION TO 37 CFR 1.121)

1. (PREVIOUSLY AMENDED) An apparatus comprising:

a first look-up-table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal;

a second look-up-table configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal; and

a logic circuit configured to generate an output signal in response to said first partial product signal and said second partial product signal, wherein said first look-up-table and said second look-up-table are implemented within a multiport memory.

2. (ORIGINAL) The apparatus according to claim 1, wherein said multiport memory comprises a dual port memory.

3. (ORIGINAL) The apparatus according to claim 1, wherein said multiport memory comprises a quad port memory.

4. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said multiport memory is selected from a group

consisting of a RAM, a ROM, a PROM, an EPROM, an EEPROM, and a flash memory ~~and other appropriate types of memories~~.

5. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first input signal is substantially equal to one of said third input signal and said fourth input signal.

6. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first input signal comprises a single-bit serial configuration.

7. (PREVIOUSLY AMENDED) The apparatus according to claim 1, further comprising:

a third look-up table configured to generate a third partial product signal from a third address formed by concatenating said first input signal and said fourth input signal.

8. (PREVIOUSLY AMENDED) The apparatus according to claim 7, further comprising:

a fourth look-up-table configured to generate a fourth partial product signal from a fourth address formed by concatenating said second input signal and said third input signal.

9. (PREVIOUSLY AMENDED) The apparatus according to claim 8, wherein said logic circuit is further configured to generate said output signal in further response to said third partial product signal and said fourth partial product signal.

10. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said logic circuit is further configured to shift said first partial product signal in response to a first shift signal before generating said output signal.

11. (PREVIOUSLY AMENDED) The apparatus according to claim 10, wherein said logic circuit is further configured to shift said second partial product signal in response to a second shift signal before generating said output signal.

12. (PREVIOUSLY AMENDED) The apparatus according to claim 1, further comprising:

a plurality of registers disposed between said first and said second look-up-tables and said logic circuit.

13. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said first partial result signal is an arithmetic function of said first input signal and said second input signal.

14. (PREVIOUSLY AMENDED) An apparatus comprising:

means for generating a first partial product signal by looking-up a first address formed by concatenating a first input signal and a second input signal to a multiport memory;

means for generating a second partial product signal by looking-up a second address formed by concatenating a third input signal and a fourth input signal to said multiport memory; and

means generating an output signal in response to said first partial product signal and said second partial product signal.

15. (PREVIOUSLY AMENDED) A method for implementing logical functions, comprising the steps of:

(A) generating a first partial product signal by looking-up an address formed by concatenating a first input signal and a second input signal to a multiport memory;

(B) generating a second partial product signal by looking-up a second address formed by concatenating a third input signal and a fourth input signal to said multiport memory; and

(C) generating an output signal in response to said first partial product signal and said second partial product signal.

16. (PREVIOUSLY AMENDED) The method according to claim 15, wherein said first partial product signal is a logical function of said first input signal and said second input signal.

17. (PREVIOUSLY AMENDED) The method according to claim 15, wherein said first input signal has a single-bit serial configuration.

18. (CURRENTLY AMENDED) The method according to claim 15, wherein said multiport memory is selected from a group consisting of a RAM, a ROM, a PROM, an EPROM, an EEPROM, and a flash memory ~~and other appropriate types of memory~~.

19. (PREVIOUSLY AMENDED) The method according to claim 15, wherein step (C) comprises the step of:

adding said first partial product signal and said second partial product signal.

20. (PREVIOUSLY AMENDED) The method according to claim 19, further comprising the step of:

shifting said first partial product signal in response to a first shift signal before adding to said second partial product signal.